What is claimed is:

1. A signal processing apparatus, comprising:

a low noise amplifier;

a mixer for mixing the signals outputted from the low noise amplifier with a local oscillation signal;

a first offset compensation amplifier for amplifying the output signals of the mixer and compensating for a DC offset existing in the output signals of the mixer firstly according to a first control signal applied thereto;

a second offset compensation amplifier connected to the output of the first offset compensation amplifier to amplify signals inputted thereto, the second offset compensation amplifier compensating for a DC offset existing in the input signals secondarily according to a second control signal applied thereto;

a variable gain amplifier for amplifying the output signals of the second offset compensation amplifier while controlling gain of the output signals;

an offset detector for detecting a DC offset existing in the output signals of the variable gain amplifier; and

an offset compensator for generating the first and second control signals to compensate for the DC offset detected by the offset detector.

2. The signal processing apparatus according to claim 1, wherein

each of the first and second offset compensation amplifiers includes each of first and second amplification elements having a gate, a drain and a source and controlling

current flowing from the drain to the source according to an input voltage applied to the gate,

first and second load impedances being respectively connected between the drains of the first and second amplification elements and a first voltage source, and

a bias current source being connected between the sources of the first and second amplification elements and a second voltage source,

wherein impedance values of the first and second load impedances are varied according to the first and second control signals applied thereto.

3. The signal processing apparatus according to claim 2, wherein

each of the first and second offset compensation amplifiers includes each of third and fourth amplification elements having a gate being respectively connected to the drains of the first and second amplification elements, a drain and a source, and outputting a voltage reduced by a voltage across the gate and source from a voltage applied to the gate to the source, and

first and second bias current sources respectively supplying variable current to the sources of the third and fourth amplification elements,

wherein the current supplied from the first and second bias current sources are varied according to the first and second control signals.

4. The signal processing apparatus according to claim 1, wherein the offset compensator includes a register and a controller, and the controller controls a data value stored in the register according to the polarity of the DC offset detected by the DC offset detector.

5. The signal processing apparatus according to claim 1, further comprising a filter for filtering a desired signal from the output signals of the first offset compensation amplifier to output the filtered signal to the second offset compensation amplifier.

6. The signal processing apparatus according to claim 5, wherein the filter is constructed such that its cutoff frequency or an order of the filter can be varied.

7. The signal processing apparatus according to claim 1, wherein the offset detector includes a comparator for comparing differential output signals of the first variable gain amplifier to each other.

8. The signal processing apparatus according to claim 7, wherein the offset detector further includes means for sampling values outputted from the comparator and outputting an average value of the sampled values.

9. The signal processing apparatus according to claim 1, wherein the offset detector further includes a filter for attenuating AC signals existing in the output signals of the variable gain amplifier to output them to the comparator.

10. The signal processing apparatus according to claim 1, wherein, in the case where the variable gain amplifier includes a plurality of variable gain amplifiers, the

offset detector detects a DC offset generated between output signals of one of the plurality of variable gain amplifiers.

11. The signal processing apparatus according to claim 1, further comprising a switch connected between the second offset compensation amplifier and the DC offset compensator.

12. The signal processing apparatus according to claim 1, wherein the register included in the DC offset compensator is a successive approximation register.

13. The signal processing apparatus according to claim 1, wherein the DC offset compensator further includes a detector for detecting a variation in the frequency of the local oscillation signal or a variation in the cutoff frequency of the filter.

14. The signal processing apparatus according to claim 4, wherein the DC offset compensator further includes a counter for increasing or decreasing the data value stored in the register according to the output value of the DC offset detector.

15. A signal processing apparatus, comprising:

a low noise amplifier;

a mixer for mixing the signals outputted from the low noise amplifier with a local oscillation signal;

a first variable gain amplifier connected to the output of the mixer, to amplify signals inputted thereto while controlling gain of the input signals;

means for eliminating a DC component existing in the output signals of the first variable gain amplifier, the means being connected to the output of the first variable gain amplifier;

an offset compensation amplifier for receiving signals that have passed the means for removing the DC component and amplifying the signals, the offset compensation amplifier eliminating a DC component existing in the accepted signals according to a control signal applied thereto;

a second variable gain amplifier for amplifying the output signals of the offset compensation amplifier while controlling gain of the output signals;

an offset detector for detecting a DC offset existing in the output signals of the second variable gain amplifier; and

an offset compensator for generating the control signal to compensate for the DC offset detected by the offset detector.

16. The signal processing apparatus according to claim 15, wherein the means for eliminating the DC component existing in the output signals of the first variable gain amplifier includes a capacitor.

17. A signal processing apparatus, comprising:

an offset compensation amplifier that differential-amplifies signals applied to its first and second input terminals to output the amplified signals to its first and second output terminals, the offset compensation amplifier compensating for a DC offset existing between signals inputted to the first and second inputs according to an offset control signal applied thereto;

a variable gain amplifier for amplifying the output signals of the offset compensation amplifier while controlling gain of the output signals;

an offset detector for detecting a DC offset existing in the output signals of the variable gain amplifier; and

an offset compensator for outputting the control signal to compensate for the DC offset detected by the offset detector to the offset compensation amplifier.

18. A method for DC offset calibration in a signal processing apparatus, comprising the steps of:

a first step of activating the signal processing apparatus;

a second step of setting initial correction data used for compensating for a DC offset;

a third step of detecting whether or not there is a variation in the frequency of a phase locked loop or a variation in the cutoff frequency of a low pass filter, the phase locked loop and the low pass filter being included in the signal processing apparatus;

a fourth step of determining from the most significant bit to the least significant bit of the correction data used for compensating for the DC offset through successive approximation to compensate for the DC offset in the case where the third step detects a variation; and

a fifth step of detecting the DC offset generated in the signal processing apparatus in real time and increasing or decreasing the correction data value according to the detected DC offset, so as to compensate for the DC offset, when the third step does not detect any variation or the fourth step is finished.

19. A method for DC offset calibration in a signal processing apparatus, comprising the steps of:

a first step of activating the signal processing apparatus;

a second step of setting initial correction data used for compensating for a DC offset;

a third step of determining from the most significant bit to the least significant bit of the correction data used for compensating for the DC offset through successive approximation, to compensate for the DC offset; and

a fourth step of detecting the DC offset generated in the signal processing apparatus in real time and increasing or decreasing the correction data value according to the detected DC offset, so as to compensate for the DC offset.